SOI CMOS for Extreme Temperature Applications

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Abstract: *A radiation-hardened SOI CMOS technology has been successfully applied to develop both analog and digital products for radiation environments. A high temperature wafer process flow has been developed by modifying this technology. The resulting wafer process is optimized for extremely wide operating temperature range rather than radiation-hardness, yet retains commonality of layout rules and the majority of manufacturing operations. The high temperature process has been used to develop standard products for wide-temperature applications (up to 225°C ambient), including an A-to-D converter, FPGA, EEPROM, and precision Opamp.*

Keywords: Radiation-hardened; High Temperature; SOI; A-to-D; Opamp; EEPROM; FPGA; Gate-array.

Introduction

Integrated circuits using SOI CMOS processes are well recognized as having structural advantages relative to bulk CMOS for certain types of radiation effects, such as Single-Event-Effects (SEE) and dose-rate phenomena. This is largely due to the reduced junction area and corresponding smaller charge collection volumes. SOI structures are also inherently superior for high temperature applications as a result of the reduced junction area, which reduces leakage currents at extreme high temperatures (up to two orders of magnitude in the range from 200° to 225°C). SOI processes may be further optimized for high temperature, for example by tailoring transistor characteristics to control MOSFET sub-threshold leakage at extreme temperatures.

Electronics are widely used in modern oil and gas exploration, drilling, and production. Data collected include heading and inclination, weight-on-bit, vibration, temperature, pressure, and radiation and resistivity of the strata. These data help operators assess drilling progress, the condition of drilling hardware, and the strata and fluids that are encountered. The single biggest obstacle for electronic data acquisition systems in very deep wells (>5,000m) is the high temperature encountered at great depth (up to 250°C). Commercial electronics are not designed for these temperatures, and conventional IC technology does not operate at these temperatures.

To promote development of deep oil and natural gas resources, the U.S. Department of Energy has co-funded initiatives with industrial partners under the Deep Trek program. These focus on development of well drilling and completion technologies operating in the high temperature (>250°C) environments of deep wells. Under this progam an SOI wafer process, along with design and simulation tools, has been developed for high temperature applications. This project also has developed high temperature components for down-hole data acquisition and control. These include a precision amplifier, a field-programmable gate array (FPGA), a high-resolution A-to-D converter, and a non-volatile memory (EEPROM). A combination of design practices and process optimization are applied to develop these SOI CMOS components capable of reliable operation over extremely wide-temperature ranges.

The technology used for the Deep Trek program has been developed by modification of a wafer process and design tools previously used for radiation-hardened digital and analog IC's. The resulting high temperature wafer process and design tools do not support radiation-hardened applications. However, completed IC layouts and masks may be used to fabricate IC's in either wafer process flow. Although results are generally design-dependent, this provides an opportunity for designs created for high temperature applications to find dual use in radiation-hardened applications, and vice-versa.

Wafer Process Adjustments for High temperature

IC Process Background and Applications: A partially-depleted, radiation-hardened SOI CMOS technology in current production has been successfully applied to develop both analog and digital products for radiation environments [1, 2]. The wafer-process is a partially-depleted 0.8 micron SOI CMOS process that employs structure and materials optimized for radiation environments. It was upgraded to production status in 1996 for digital applications, primarily digital ASICs and radiation-hardened SRAM's. This technology has proven reliability for aerospace applications. More recently radiation-hardened analog / mixed-signal IC's have been developed (for example, a 12-bit, 20MSample per second A-to-D converter).

High temperature IC Process Technology: A high temperature wafer process flow has been developed by modifying the above radiation-hardened SOI process [3]. The resulting wafer process, although no longer radiation hardened, is optimized for extremely wide operating temperature range. Commonality of layout rules with the radiation-hardened process is retained, along with usage of common process equipment and manufacturing procedures.

The high temperature process objective is to fabricate commercial integrated circuits for extreme temperature operation (from -55°C to 225°C). Commercial applications for this temperature range include sensor interface electronics and distributed controls for aircraft, down-hole oil and gas exploration and production management, industrial process controls, power-management, and internal combustion engine sensor interfaces [4-7]. Radiation-hardening is not considered a primary technology criterion for these applications.

Manufacturing process optimization for high temperature includes elimination of radiation-hardening process steps for commercial markets, and adjustment of threshold implants to reduce sub-threshold leakage at high temperatures. Both high temperature and radiation-hardened processes include devices that support analog as well as digital applications. Features of the High Temperature SOI (HTSOI) process are listed in Table 1.

Table 1: High Temperature SOI Process Features

Process Feature	**Typical Characteristics**
Gate Oxide thickness	150 angstroms
Minimum transistor length	0.8 microns
Max. Gate Oxide Voltage	5.25V
Target Vtn/Vtp 25°C 250°C	 1.2V / -1.3V 0.85V / - 1.0V
Sub-Vt slope (mV/dec) 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor “Off current” Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width
# of metal layers	3 or 4
Top Silicon Thickness	0.2 microns
Buried Oxide Thickness	0.4 microns
Poly-silicon resistors	90 ohms per square, 415 ppm/°C
CrSiN resistors	2.5K ohms per square, ± 300 ppm/°C
Linear Capacitor	670 angstroms, <150 ppm/Volt

The HTSOI wafer process used by the Deep Trek program is layout-rule and photo-mask compatible with Honeywell’s military temperature range aerospace technology. This has made it possible to leverage previously developed ASIC platforms and design processes. An HTSOI gate-array digital cell library has been fully characterized for operation over the -55°C to +250°C temperature range. Available high temperature gate-array platforms are summarized in Table 2.
The high temperature and radiation-hardened versions of this SOI process are layout and mask compatible. This means that a design targeted for application to either the radiation-hardened or high temperature versions of the process can be fabricated in either flow. This has enabled the development of high temperature products derived from layouts that were originally developed for natural space applications, for example a 32K x 8 bit high temperature SRAM [8].

Table 2: High temperature ASIC Features

Gate-Array Product	Total Gates	Maximum Packaged Signal I/O	Usable Gates
HT2080	84,512	172	72,000
HT2160	159,528	240	126,000
HT2300	295,392	320	216,000
HT2400	389,120	320	275,000

High Temperature Design Considerations

High temperature electro-migration (E-M) considerations are addressed by management of current-density in on-chip conductors, either through de-rating of operating frequency (for digital applications) or through high temperature optimized interconnect layout (primarily power bus and/or DC output conductors). Temperature-compensated biasing techniques for analog circuits are employed to maintain gain and bandwidth over an extremely wide temperature range. Design toolkits have been updated and applied for high temperature applications [9]. These include development of SPICE models and timing libraries applicable from -55°C to 250°C. Laser-trimming and high temperature wafer probing can be combined to adjust voltage reference temperature coefficients, or for tailoring other temperature-dependent circuit performance.

Deep Trek High Temperature IC Components

High temperature components have been developed under the Deep Trek program [10] using the high temperature design and wafer process (see Figure 3).

High Temperature Dual Precision Amplifier: The high temperature dual precision amplifier has been fully verified at 225°C with additional testing up to 375°C [11]. Offset voltage vs. common-mode input voltage is shown in Figure 2 (data courtesy of Randy Normann, Sandia National Lab).

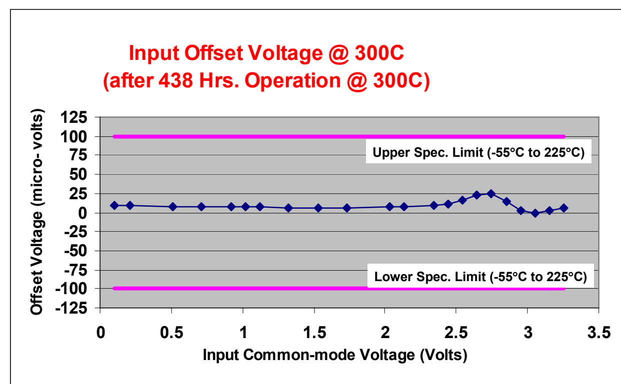

Figure 2: Amplifier Offset at 300°C

High Temperature FPGA: The Deep Trek FPGA was developed as a licensed functional equivalent to a commercial FPGA, the Atmel AT6010. It is a re-programmable, SRAM-based FPGA that provides up to 32,000 logic gates and 204 I/O. It has been fully verified by wafer-probe testing at 200°C. A full-custom design process was used. The design includes over 3 million transistors. Leakage current at 200°C is under 0.5mA.

High Temperature ADC: The Deep Trek high temperature ADC targets 18-bit resolution at 100 samples/sec. It uses a second-order sigma-delta modulator with 204.8 KHz sampling clock. Digital filtering and control logic was synthesized from Verilog code and implemented using a high temperature gate array design process. Analog circuits were designed and laid out as a full-custom block dropped into the HT2000 digital gate-array I/O frame. Test results include 17.4 bits of resolution at 225°C. The ADC on-chip voltage reference has been tested up to 275°C (see Figure 2).

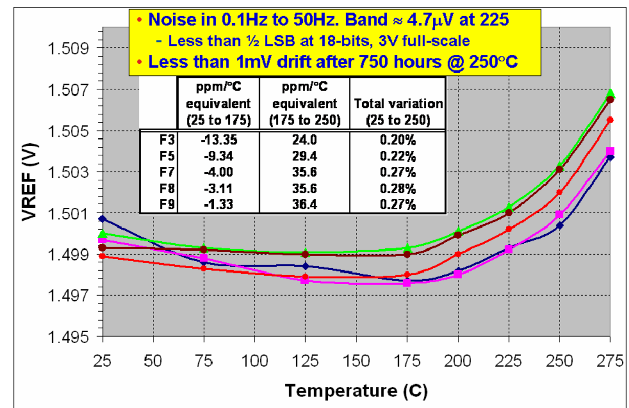

Figure 2 ADC Voltage Reference Performance (5 units)

High Temperature EEPROM: The Deep Trek high temperature non-volatile memory (EERPOM) uses a single-poly floating gate memory cell that is programmed and erased via Fowler-Nordheim tunneling. This approach required no additional process steps. A 4K x 8 bit demonstration memory has been fabricated and verified for operation up to 250°C. A 32K x 8 design that can be operated in both parallel and serial mode is in progress.

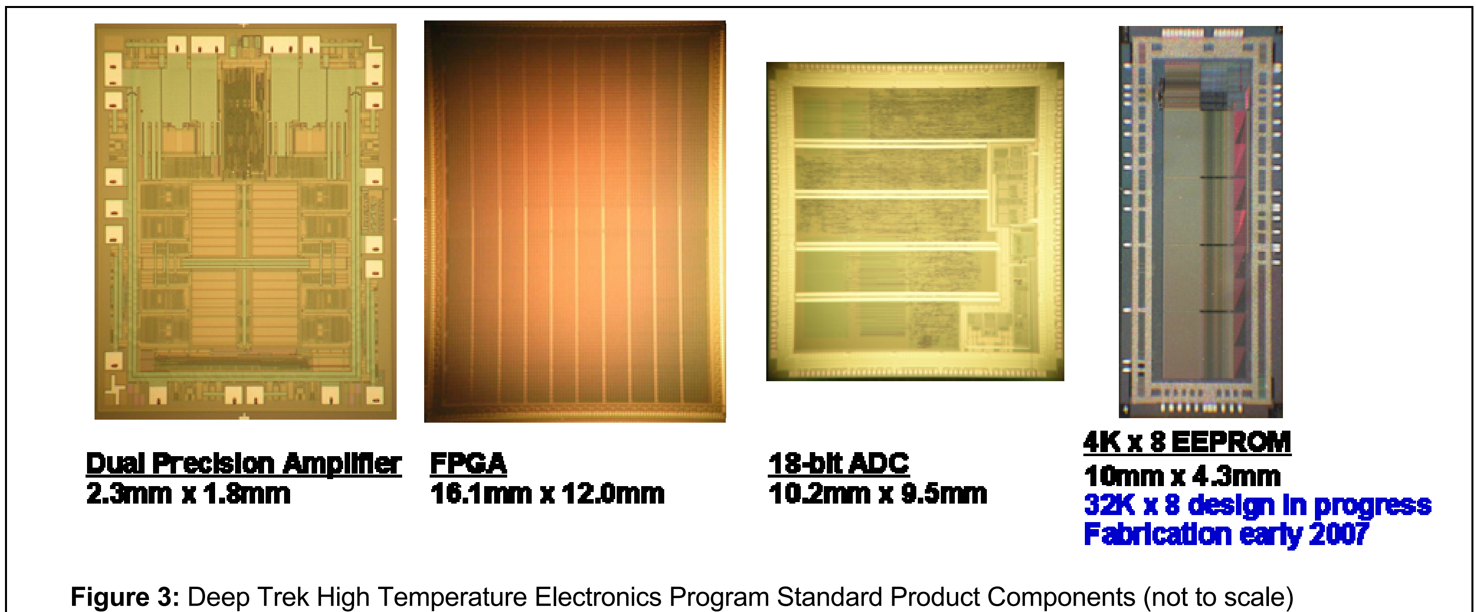

Figure 3: Deep Trek High Temperature Electronics Program Standard Product Components (not to scale)

Dual Use Potential

The wafer-process technology for high temperature described herein is distinct from previously developed radiation-hardened technology. Transistor characteristics are not the same in these two processes, although IC designs and masks are developed using a common set of layout rules. It is therefore possible to use a common mask set to fabricate integrated circuits in either process flow (radiation-hardened or high temperature). Designs developed for a radiation-hardened application may thereby be built for a high temperature application, and vice versa as long as performance objectives are appropriately adjusted. This approach has been successfully employed to provide a high temperature 32K x 8 SRAM using layouts originally developed for a 1MRad (Si) total-dose radiation-hardened SRAM. This can also work in the reverse (i.e., using a high temperature design and fabricating it in the radiation-hardened process flow). As an example, consider the Deep Trek high temperature precision amplifier. This circuit has been simulated at up to 150°C using simulation models corresponding to the radiation-hardened process (Figure 4). These results show that good performance can be obtained by this design in either process flow.

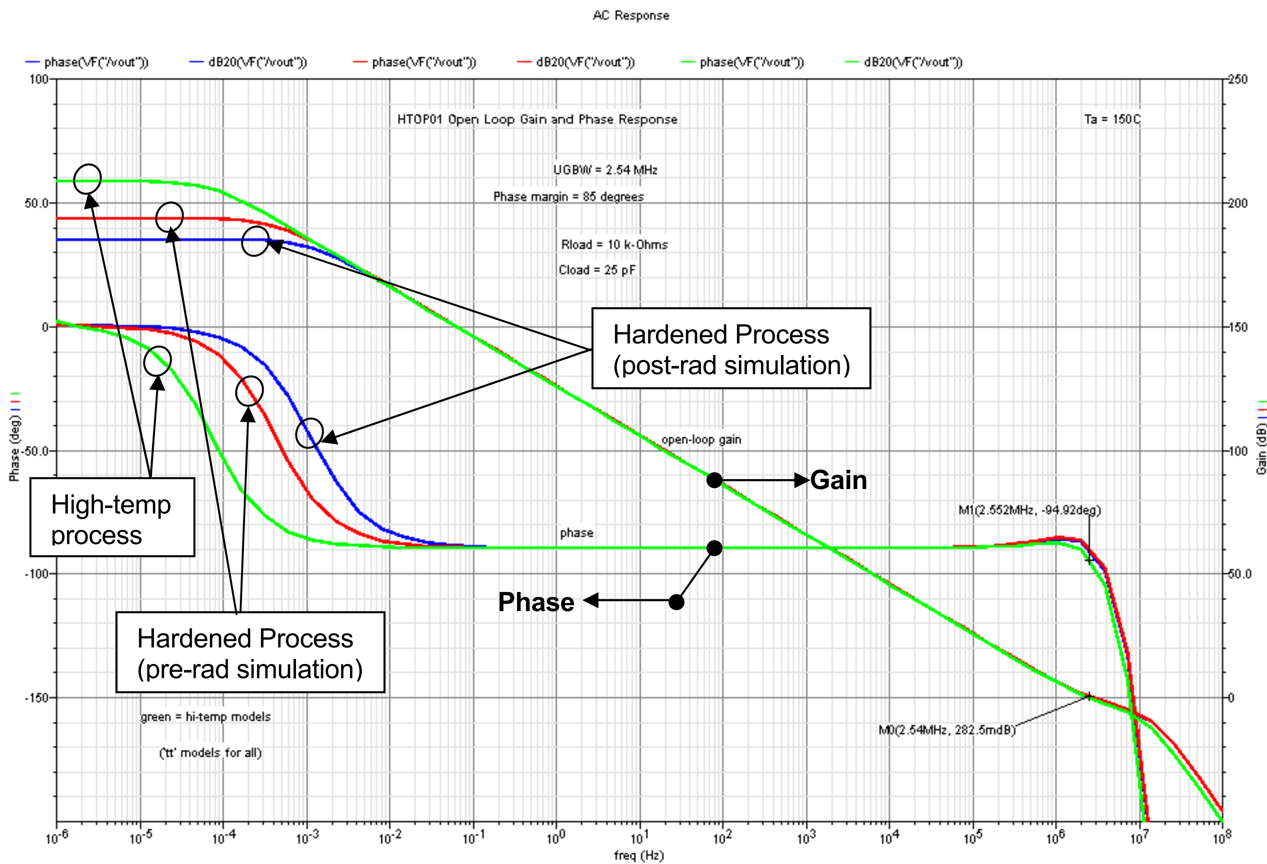

Figure 4: High Temperature Op-amp Simulated AC Response; High Temperature Versus Hardened Process Flow

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